

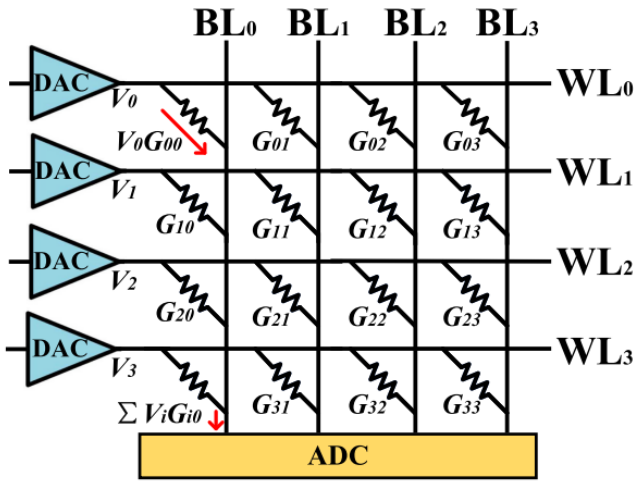
ReRAM Compute Asic Fabrication – Project Plan

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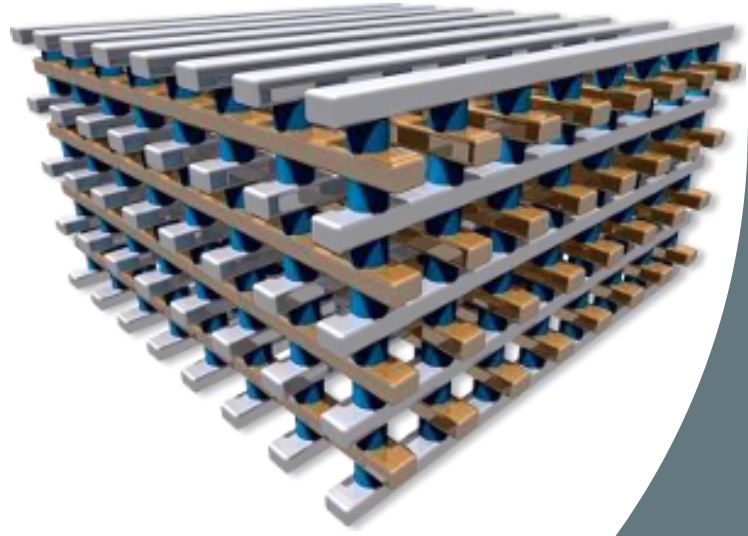
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Our Project

- Resistive RAM (ReRAM) crossbar that can perform computations in the analog domain
- Requires less energy and data transfers then typical memory
- Input taken from a digital system, calculations done in analog domain, and output sent to a digital system
- Easily perform matrix vector multiplication in one step
- Test-bed for different configurations and characterization



[1]



[2]

1. Jiahong Xu, Haikun Liu, Xiaoyang Peng, Zhuohui Duan, Xiaofei Liao, and Hai Jin. 2024. A Cascaded ReRAM-based Crossbar Architecture for Transformer Neural Network Acceleration. ACM Trans. Des. Autom. Electron. Syst. 30, 1, Article 10 (January 2025), 23 pages. https://doi.org/10.1145/3701034

2. https://www.crossbar-inc.com/technology/reram-overview/

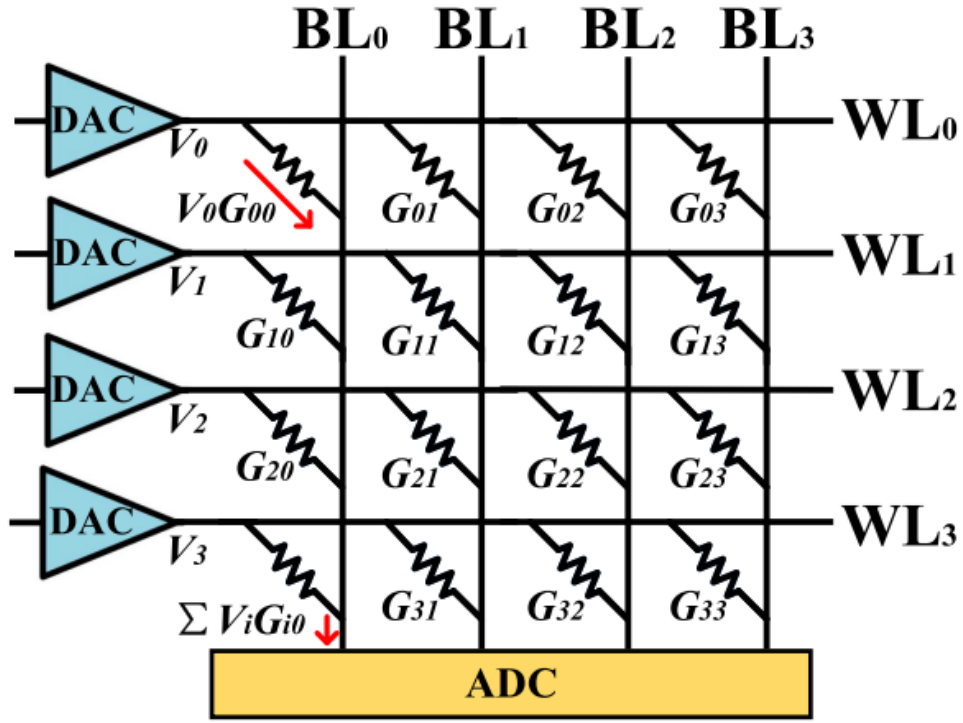
Management Style

Waterfall Style

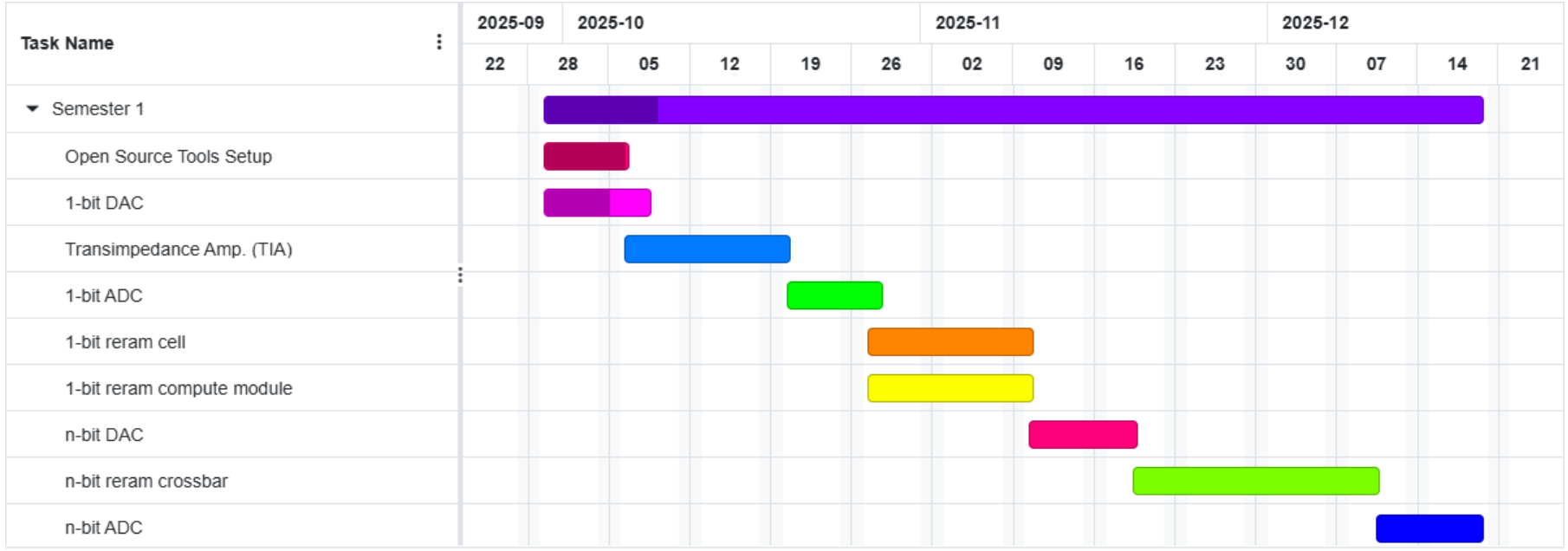
- Lots of sequential components
- Can complete some components in parallel, then connect them up for the final product
- Every individual component needs at least four steps in the design process:
  - Schematic
  - Testbench
  - Layout
  - Post-layout characteristics

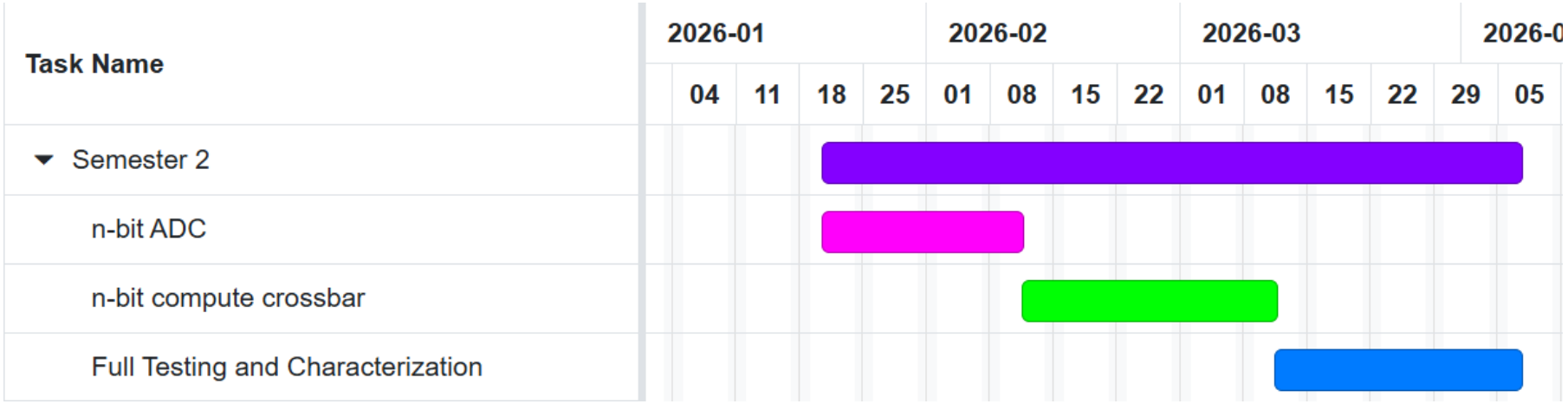
Task Decomposition

- Digital to Analog Converter
- ReRAM Crossbar
- Transimpedance Amplifier
- Analog to Digital Converter
- Full Integration of Modules



Gantt Chart and Personal Effort Requirements

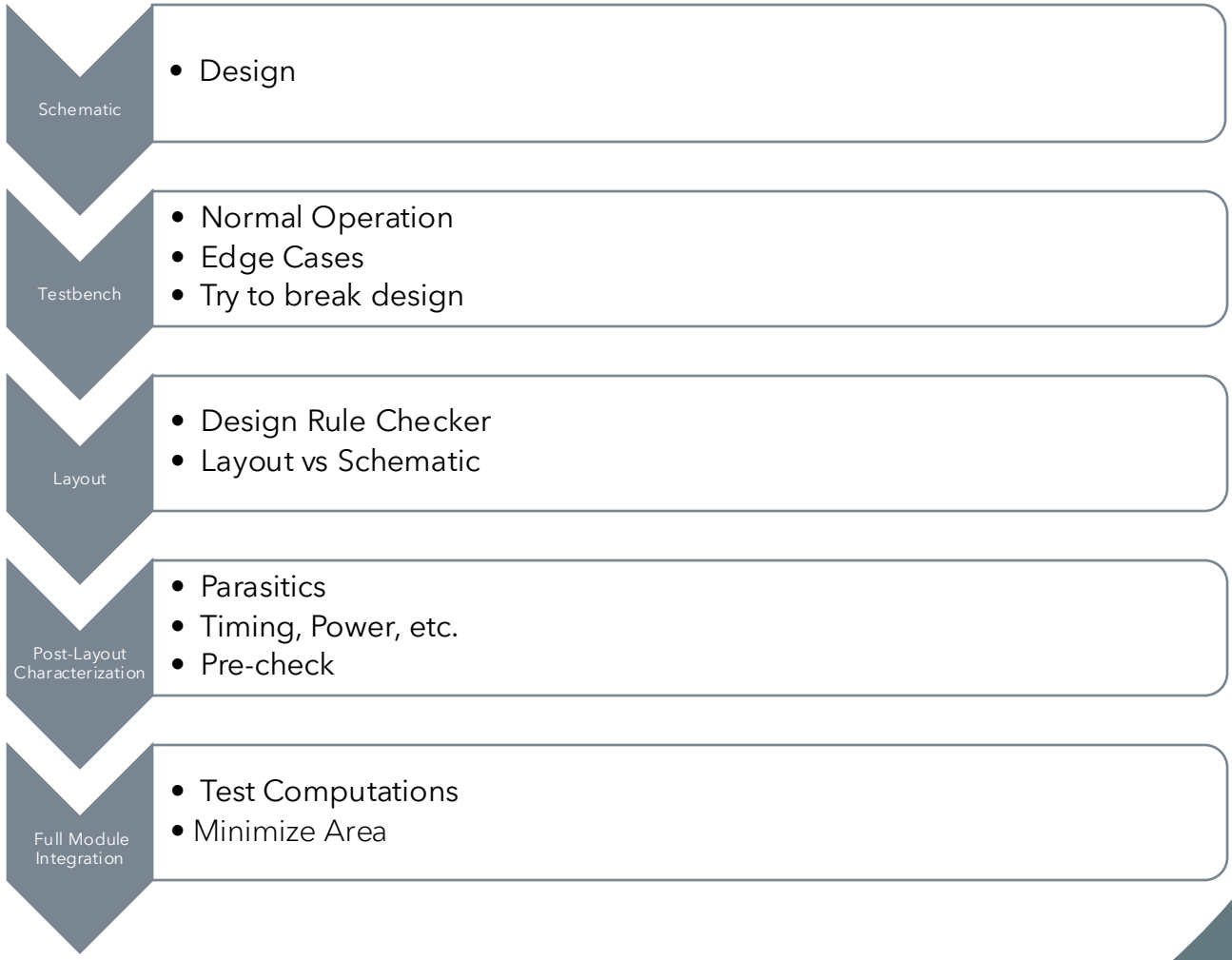




- Expectation of 8 hours/person/week of work
- 1 – 3 weeks per task
- 2-3 days per intermediate milestone
- Estimates are generous

Milestones

- DAC
  - 1 bit
  - Eventually 4 bit
- Transimpedance Amplifier
  - >10dB Gain
  - Low noise
- ADC
  - > 10MHz sampling rate
  - Linear output
  - 4-bit later?
- ReRAM Crossbar
  - 1x1
  - Goal: 4x4
- Complete Design
  - ~100ns input to computed value



Risks and Risk Mitigation

Compute Failure

- Risk (EXTREME): unable to compute matrix-vector product correctly
- Sequential nature exacerbates this problem
- Noise
- Variation tolerance

High risk of time delays due to nature of tools being used

Mitigation Plan

- Redundancy built-in to design
- Individual modules for characterization
- Route multiple outputs for measurement between components
- Communicate with ChipForge members on tools and processes

Questions?